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Esposito, B.; Fortuna, L.; Rizzo, A.;
Neural Networks, 2004. Proceedings. 2004 IEEE International Joint Conference on
Volume 4, 25-29 July 2004 Page(s):2931 - 2936 vol.4
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2. **A neural system for radiation discrimination in nuclear fusion applications**
Esposito, B.; Fortuna, L.; Rizzo, A.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on
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3. **Neutron emission profiles measurements from the FTU Tokamak neutron collimator diagnostic**
Bertalot, L.; Esposito, B.; Batistoni, P.;
Plasma Science, 1999. ICOPS '99. IEEE Conference Record - Abstracts. 1999 IEEE International Conference on
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Soderstrand, M.A.;
Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on
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2. **Highly efficient, limited range multipliers for LUT-based FPGA architectures**
Turner, R.H.; Woods, R.F.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 12, Issue 10, Oct. 2004 Page(s):1113 - 1118
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3. **Novel CSD-based digital heterodyne circuit**
Soderstrand, M.A.; Cho, G.Y.;
Signals, Systems and Computers, 2003. Conference Record of the Thirty-Seventh Asilomar Conference on
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4. **MSDCT Architecture Implementation with DA Based Optimized LUT**
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5. **Comparison of RNS and optimized FIR digital filters in Xilinx FPGA's**
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Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on
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6. **Multi-layer perceptrons with discrete weights**

Marchesi, M.; Orlandi, G.; Piazza, F.; Pollonara, L.; Uncini, A.;
Neural Networks, 1990., 1990 IJCNN International Joint Conference on
17-21 June 1990 Page(s):623 - 630 vol.2
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7. **Comparison of low complexity clipping algorithms for OFDM**
Hill, G.; Faulkner, M.;
Personal, Indoor and Mobile Radio Communications, 2002. The 13th IEEE International Symposium on
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Inventor Information for 10/829559

Inventor Name	City	State/Country
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Last Name = HAZANCHUK
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Application#	Patent#	Status	Date Filed	Title	Inventor Name
08027666	5537564	150	03/08/1993	TECHNIQUE FOR ACCESSING AND REFRESHING MEMORY LOCATIONS WITHIN ELECTRONIC STORAGE DEVICES WHICH NEED TO BE REFRESHED WITH MINIMUM POWER CONSUMPTION	HAZANCHUK, ASHER
09863650	7058675	150	05/22/2001	APPARATUS AND METHOD FOR IMPLEMENTING EFFICIENT ARITHMETIC CIRCUITS IN PROGRAMMABLE LOGIC DEVICES	HAZANCHUK, ASHER
09891710	Not Issued	41	06/26/2001	Parallel samples, parallel coefficients, time division multiplexing correlator architecture	HAZANCHUK, ASHER
10326652	6888372	150	12/20/2002	PROGRAMMABLE LOGIC DEVICE WITH SOFT MULTIPLIER	HAZANCHUK, ASHER
10668449	6943579	150	09/22/2003	VARIABLE FIXED MULTIPLIERS USING MEMORY BLOCKS	HAZANCHUK, ASHER
10829559	Not Issued	30	04/22/2004	Method and apparatus for implementing a multiplier utilizing digital signal processor block memory extension	HAZANCHUK, ASHER
11168984	Not Issued	61	06/27/2005	Variable fixed multipliers using memory blocks	HAZANCHUK, ASHER
11264778	7124161	150	10/31/2005	APPARATUS AND METHOD FOR IMPLEMENTING EFFICIENT ARITHMETIC CIRCUITS IN PROGRAMMABLE LOGIC DEVICES	HAZANCHUK, ASHER
11477759	Not Issued	41	06/29/2006	Method and systems to align output signals of an analog-to-digital converter	HAZANCHUK, ASHER
11504849	Not Issued	20	08/16/2006	Apparatus and method for implementing efficient arithmetic circuits in programmable logic devices	HAZANCHUK, ASHER
11830807	Not Issued	19	07/30/2007	VARIABLE FIXED MULTIPLIERS USING MEMORY BLOCKS	HAZANCHUK, ASHER
60236244	Not Issued	159	09/28/2000	Apparatus and method for implementing complex arithmetic circuits in programmable logic devices	HAZANCHUK, ASHER

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10668449	6943579	150	09/22/2003	VARIABLE FIXED MULTIPLIERS USING MEMORY BLOCKS	ESPOSITO, BENJAMIN
10712500	7269617	150	11/12/2003	HYBRID MULTIPLIERS IMPLEMENTED USING DSP CIRCUITRY AND PROGRAMMABLE LOGIC CIRCUITRY	ESPOSITO, BENJAMIN
10821377	Not Issued	41	04/09/2004	Maintaining data integrity for extended drop outs across high-speed serial links	ESPOSITO, BENJAMIN
10829559	Not Issued	30	04/22/2004	Method and apparatus for implementing a multiplier utilizing digital signal processor block memory extension	ESPOSITO, BENJAMIN
10922628	Not Issued	30	08/19/2004	Memory configured for multi-channel multiplication	ESPOSITO, BENJAMIN
11168984	Not Issued	61	06/27/2005	Variable fixed multipliers using memory blocks	ESPOSITO, BENJAMIN
11323387	Not Issued	30	12/29/2005	High-speed FIR filters in FPGAs	ESPOSITO, BENJAMIN
11820268	Not Issued	17	06/18/2007	Multichannel memory-based numerically controlled oscillators	ESPOSITO, BENJAMIN
11830807	Not Issued	19	07/30/2007	VARIABLE FIXED MULTIPLIERS USING MEMORY BLOCKS	ESPOSITO, BENJAMIN
10804294	Not Issued	41	03/18/2004	Efficient implementation of multi-channel integrators and differentiators in a programmable device	ESPOSITO, BENJAMIN J.

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